# **CSE 620: Advanced Computer Architecture**

# **Project: HDL Test bench**

**Digital System Modeling using HDL**

**ALU Test bench**

**Deliverables:**

1. **Design example name and location in the slides**

Design Example name: ALU.

Location: Example 8, page 13-14, VHDL Combinational logic modeling slides.

The code is converted to Verilog and attached.

1. **Test strategy**
2. Manually setting the two operands (A and B) to certain values (in our case 4 and 6 respectively)
3. Observing the output (C) which represents the operations done in an orderly fashion (add, subtract, multiply and division) and then compare between the actual and expected results.
4. Expected results: 6, 2, 8, 2

Actual results: 6, 2, 8, 2

1. The expected and actual are the same, thus verifies the functionality/behavior of the design.
2. **Simulation results**

Refer to the file name: “ALUTestBench.bmp”

1. **Names of all used tools**

ModelSim PE student edition

***End of Assignment***